Abstracts

High-Q capacitors implemented in a CMOS process for low-power wireless applications

C.-M. Hung, Y.-C. Ho, I.-C. Wu and K. O. "High-Q capacitors implemented in a CMOS process for low-power wireless applications." 1998 Transactions on Microwave Theory and Techniques 46.5 (May 1998, Part I [T-MTT]): 505-511.

In a foundry 0.8-/spl mu/m CMOS process, low-cost capacitors with a measured Q factor of around 50 at 3 GHz and high intrinsic capacitance/area (/spl sim/200 nF/cm/sup 2/) were demonstrated. When extrapolated to 900 MHz, the Q factor is greater than 100. The capacitors use a poly-to-n-well MOS structure which has been commonly dismissed for high-Q applications due to the high n-well sheet resistance (/spl sim/1 k/spl Omega///spl square/). Utilizing the structure, a low-noise amplifier (LNA) with a resonant frequency of 960 MHz, power gain of 16.2 dB, 1-dB compression point (P/sub 1 dB/) of -5 dBm, and noise figure of 3.5 dB was demonstrated. Using a rule of thumb, the third-order harmonic intercept point (P/sub IP3/) was estimated to be 5 dBm from the P/sub 1 dB/ data. Despite concerns for nonlinearity of the capacitors, these results suggest that this capacitor structure could be used in LNA's with a large dynamic range.

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